MICROMACHINED STIMULATING ELECTRODES

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Solid-State Electronics Laboratory
Bioelectrical Sciences Laboratory
Department of Electrical Engineering and Computer Science
University of Michigan
Ann Arbor, Michigan
48109-2122

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MICROMACHINED STIMULATING ELECTRODES

Summary

During the past quarter, we began final layout on a new set of passive recording and stimulation probes for use by external and internal personnel. These include probes for penetration studies aimed at optimizing probe tip shape to minimize penetration forces and resulting tissue damage along the electrode track. Using a combination of a deep boron diffused shank and a shallow-diffused tip, we have demonstrated the ability to form nearly ideal tips that approach the sharpness of the defining masks.

All of the problems revealed in testing the recent run of STIM-1 active probes have been corrected with simple process changes with the exception of the background currents noted on these devices. Extensive tests have been carried out to quantify and explain these currents. Both lateral and vertical parasitic bipolar transistors have been found to generate these currents in processes using moderately deep p-wells together with 10μm epitaxial thicknesses. It appears that reducing the p-well depth and increasing the epi thickness to 16μm will correct these problems, and we are currently seeking to confirm this conclusion prior to another run of these probes.

The circuitry for a second-generation active probe (STIM-2) has been fabricated in a commercial foundry (MOSIS/Orbit) and has been tested. All of the circuitry is fully functional and appears to work as intended. This probe provides the ability to select eight of 64 output sites and generates drive currents for the selected sites with a range from -127μA to +127μA with a current resolution of 1μA. The circuitry operates from ±5V supplies and uses a 4MHz input clock. The external circuitry for driving these active probes has also been modified to accommodate both generations of the active devices.

During the coming term, the new passive probes will be fabricated and the penetration studies will be started. In addition, additional testing will be performed on STIM-1 and layout will be completed on STIM-2 so that the fabrication of these probes can begin during the latter part of the summer.

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1. Introduction

The goal of this research is the development of active multichannel arrays of stimulating electrodes suitable for studies of neural information processing at the cellular level and for a variety of closed-loop neural prostheses. The probes should be able to enter neural tissue with minimal disturbance to the neural networks there and deliver highly-controlled (spatially and temporally) charge waveforms to the tissue on a chronic basis. The probes consist of several thin-film conductors supported on a micromachined silicon substrate and insulated from it and from the surrounding electrolyte by silicon dioxide and silicon nitride dielectric films. The stimulating sites are activated iridium, defined photolithographically using a lift-off process. Passive probes having a variety of site sizes and shank configurations have been fabricated successfully and distributed to a number of research organizations nationally for evaluation in many different research preparations. For chronic use, the biggest problem associated with these passive probes concerns their leads, which must interface the probe to the outside world. Even using silicon-substrate ribbon cables, the number of allowable interconnects is necessarily limited, and yet a great many stimulating sites are ultimately desirable in order to achieve high spatial localization of the stimulus currents.

The integration of signal processing electronics on the rear of the probe substrate (creating an "active" probe) allows the use of serial digital input data which can be demultiplexed onto the probe to provide access to a large number of stimulating sites. Our goal in this area of the program has been to develop a family of 16-site active probes capable of chronic implantation in tissue. For such probes, the digital input data must be translated on the probe into per-channel current amplitudes which are then applied to the tissue through the sites. Such probes require five external leads, virtually independent of the number of sites used. As discussed in our previous reports, we have defined three probes which represent the first-generation of these active stimulating devices and have designated them as STIM-1, -1a, and -1b. All three probes provide 8-bit resolution in setting the per-channel current amplitudes over the biphasic range from 2μA to ±254μA; however, the probes differ markedly in the number of sites that can be active at any one time. STIM-1 offers the ability to utilize all 16 sites independently and in parallel, while -1a allows only two sites to be active at a time (bipolar operation), and -1b is a monopolar probe, allowing the user to guide an externally-provided current to the site selected by the digital address. The circuit complexity among these designs spans an order of magnitude in device count, ranging from a 400 transistors (STIM-1b) to over 7000 transistors (STIM-1). The high-end STIM-1 contains provisions for numerous saftey checks and for features such as remote impedance testing in addition to its normal operating modes.

During the past quarter, research on this contract has focused on four areas. A variety of new passive probes are being designed for both external and internal users, including a series of designs for penetration studies as described below. These penetration studies will help in determining the optimum tip shape for minimum tissue damage and maximum ease of penetration. Further tests were also performed last term on the first active stimulating probes we have processed (STIM-1), and the circuitry for a second-generation series of active probes (STIM-2) has been fabricated in a commercial foundry

(MOSIS) and tested. Finally, the external electronics for STIM-1 has been modified to make it functional with both STIM-1 and STIM-2. These activities are described in the sections below.

2. *Passive Stimulating Electrode Development*

During the past quarter, two additional fabrication runs of passive probes have been performed using mask sets generated previously. In general, these runs were successful although some continuing problems are being experienced with iridium adhesion in the pad areas. This is attributed to stress in the as-deposited films. The thickness of the titanium undercoat will be increased to assess its effect on this problem. It is also true, however, that on many of our new probes the pads are being implemented in gold to make them easier to bond by external users, so this may also avoid the problem.

We are now completing the design of three new mask sets of probes for both internal and external users. These masks include both recording and stimulating designs, including probes for Huntington (Agnew) and Rutgers (Buzsaki). Also included are probes for the penetration studies described below. We expect these probe designs to be completed and fabricated during the coming term.

We have also been developing software and electronics to support several passive stimulation probe experiments that will be run at the Kresge Hearing Research Institute (KHRI) this summer. LabView, a software development system developed by National Instruments, is being used to generate the necessary programs to accomplish the experiments. These functions include waveform generation, stimulus presentation, and data acquistition. The programs are run on a Macintosh Quadra 950. The electronics that provide the interface between the Mac and the probe have been designed and are being constructed on-site. The electronics feature a constant current source for stimulation signals and feedback of both the signal input into the probe and the IR drop across the probe. Also, isolator circuits have been incorporated into the electronics to eliminate ground loop currents. Battery power is used where necessary to improve isolation. Finally, the same circuit can be configured such that it can perform probe characterization in-vitro, similar to the impedance test station in EECS. In fact, the user interface for the KHRI impedance test station will be identical to that in EECS, as LabView is used for both.

The experiments that will employ the above system were described in detail in the last quarterly report. Two probe designs (also described in the last report) will be used for IR drop studies with chronically implanted electrodes. Several stimulus current intensities will be passed between probe sites of varying size. The IR drop across the sites will be measured to determine the effect of above parameters on tissue conduction. In addition, stimulation of sites both between and along shanks will be studied to determine if differences in tissue condition between sites affects the probe recording properties. Histology will be performed several weeks after conclusion of the experiments. Finally, we will attempt to determine the path of current flow around the probes by using the neuronal activity marker c-fos.

3. *Penetration Studies*

During the past quarter, we began layout of a series of probes designed to study the insertion forces and tissue damage associated with probe insertion through the pia

arachnoid and dura mater in guinea pigs, rats, and perhaps primates. The optimal probe tip shape should allow ease of penetration with minimal dimpling of the cortical surface, minimize tissue damage and reaction along the track, and permit a high degree of probe-tissue coupling for effective recording and stimulation. The tips shown in Fig. 1, repeated from the previous quarterly report, illustrate some of the basic geometries that will be studied as realized using combinations of (nearly) isotropic boron diffusion, wet silicon etching in EDP, and selective dry etching. The wet etch will stop when the boron concentration in the silicon substrate exceeds about 5 x $10^{19}cm^{-3}$, whereas the dry etches are largely insensitive to doping. The simple diffused tip shown in the upper left in the figure results from diffusion only. In contrast, when the boron diffusion is allowed to be much wider than the intended probe, anisotropic RIE-based dry etching can be used to slice through this layer resulting in a probe of nearly constant thickness and a rather chisel-shaped profile as in the upper right. RIE can also be used to produce sloped sidewalls. As we have considered the process for these "chisel" tips in more detail, it has been recognized that these tips may be more difficult to fabricate and may complicate the probe fabrication process significantly. This is due to the rather low etch selectivity available from dry etching processes. In order to etch through more than 15μm of silicon in addition to the field dielectrics, it may be necessary to employ an aluminum mask on top of the probe instead of the normal photoresist layer. This then would require the use of a layer (e.g., of photoresist or dielectric) between the aluminum and the sites to prevent metallic intermixing and site contamination. This, in turn, requires a rather complex lithography sequence that may not be worth it unless these sorts of tips exhibit substantial advantages, which we frankly do not anticipate. Thus, these chisel tips will be attempted first using relatively small process changes (e.g., multiple resist masks and a two-step sequential etch process) and we will move to a full chisel process only if they appear significantly advantageous. Finally, as shown at the bottom in Fig. 1, the boron etch-stop can be combined with RIE to produce a more needle-shaped tip. Here, the tip narrows sufficiently that the boron diffusion transistions from a full area source to a line source, with a corresponding decrease in the diffusion depth as we approach the tip. The effect is to markedly taper the silicon substrate depth as we approach the tip after EDP etching. RIE can still be used on the sidewalls to decrease their rounding or the rounding there can be retained.

During the past quarter, we have developed another way to produce sharp tips that is more easily process compatible with the normal probe process. In fact, the approach requires no additional masks or process steps beyond the standard process and was mentioned in the previous quarterly report. On all of our chronic probes, we now include a built-in silicon ribbon cable to provide leads between the probe and the percutaneous plug. This cable is fabricated using a shallow boron diffusion to form a flexible back-plate for the cable. The same shallow diffusion can be used at the tip of the probe, however, in order to form a sharp point there. In this approach, the deep boron diffusion (15μm) is still used for the shank (to give it the required stiffness) but over a short distance at the tip a shallow diffusion (3μm) is used to extend the shank and form a tip sharp enough for easy penetration of the tissue. Since the tip diffusion is shallow, the lateral diffusion is limited to typically ≤2μm. Thus, the tip retains most of the shape of the mask.

Figure 2 shows top views of the probe tip and compares the use of a deep boron diffusion only (case 1) with the combination of a deep shank diffusion and a shallow tip diffusion (case 2). In a third case, the shallow boron diffusion at the tip is replaced by an ion implantation step, although in this case the boron level would be shallower still and probably not deep enough to give the required strength or etch-stop. These approaches have been explored in an effort to form tip angles of <20° on test substrates, two of which are shown in Fig. 3. The upper photo here shows a probe tip produced using only a deep diffusion, whereas the lower photo shows a probe produced using a deep diffusion for the

shank and a shallow diffusion for the tip. Figure 4 shows an SEM view of the cross-section (thickness) of this last probe. The boron diffusions result in a very gradual taper in thickness from the tip area to the thicker shank and appear to be nearly ideal. Note that at the very tip of this probe, the thickness tapers to a point as the result of both the boron diffusion characteristics and the segregation of boron into the upper masking oxide.

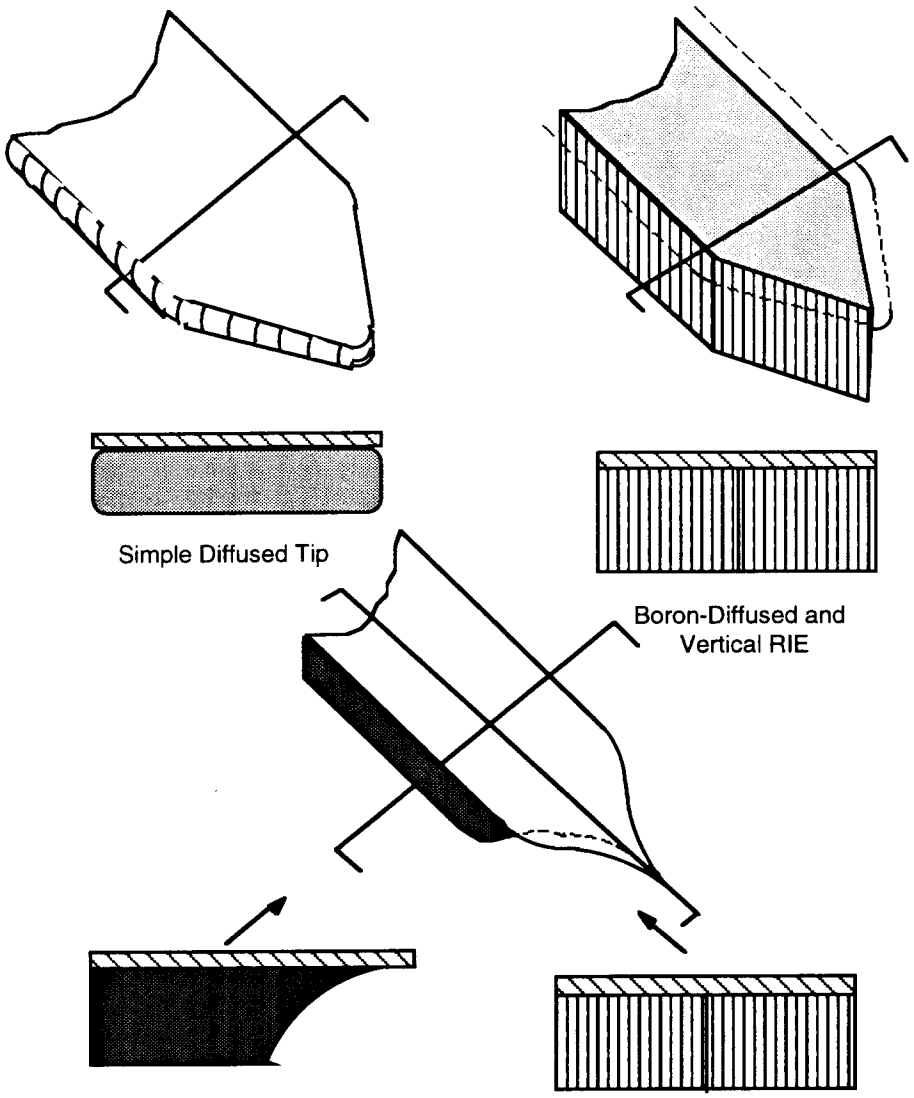


Fig. 1: Tip geometries realizable using combinations of boron-diffused etch-stops, wet etching of the silicon substrate in EDP, and dry etching using RIE. Upper left: deep boron diffusion and wet etch; upper right: deep boron diffusion and dry etch (RIE) to shape the sidewalls; lower center: deep diffusion with a more sharply tapered tip with a possible dry etch for the sidewalls.

The probes being designed for penetration studies will have three tip angles (20°, 33°, and 45°) and will be fabricated in both single- and multiple- (10) shank designs. Both deep boron diffusions alone and combined deep and shallow diffusions will be used, with RIE etching of the sidewalls a further process option. In the case of a shallow tip diffusion, RIE could be used to sharpen the diffusion sidewalls since they are not very deep and hence high selectivity with the masking material would not be required. These probes include strain gauges at the bases of the shanks to measure the penetration force. They also contain four-electrode structures for monitoring the tissue resistivity near the probe shank in hopes of obtaining some indication of the tissue damage being created by the insertion process. As part of the design of these probes, the probe, fluid pool along the shank, and the tissue were modeled with circuit elements and simulations were run using SPICE while varying the fluid pool thickness and the stimulation and recording site separations. This was done to find the best separation of the recording and stimulation sites on the probe shank, which is characterized by the greatest observable change in resistance due to changing the fluid pool thickness. As a result of these simulations, the stimulation and recording sites were arranged in the layout with 150μm and 50μm separations, respectively. One four-point-electrode probe was included in the layout with a 90° ribbon cable to allow for chronic observation of the tissue resistivity. It is expected that there is initial fluid pooling around the probe shank, which is then reabsorbed by the tissue as the wound heals.

The layout of the *artificial neuron* probe pictured in the previous report for the investigation of long-term recording degradation has also been completed. In addition to recording from active driven neurons in the CN, this probe will allow the insertion (via the stimulating sites) of signals that can be monitored on the recording sites throughout the life of the implant so that tissue encapsulation of the recording sites can hopefully be distinguished from changes in local neuronal activity. During the coming quarter, it is expected that these probes will be fabricated and tested; the strain gauges will be calibrated; and the acute and chronic studies will begin.

4. *Development of Active Stimulating Probes*

As discussed in previous quarterly reports, the circuitry for our first-generation active stimulating probes (STIM-1, -1a, -1b) has been fully verified via simulation and via fabrication in a commercial foundry (MOSIS). This circuitry meets all of the design goals for such circuits, offering 16-channels of stimulation with 8-bit resolution in current over a range from zero to ±254μA. The circuits run from a 4MHz clock, allowing the current on any channel to be altered within 4μsec, which is fast enough to be virtually simultaneous to the tissue. The processing problems associated with integrating this circuitry onto probes have been solved with the use of aluminum circuit interconnect with an overlayer of low-temperature oxide (LTO). In chronic use this would typically be covered by PECVD nitride, by a metal shield layer, and by a polymer. These would act as additional chemical barriers and as an optical shield. Probes have been implemented in monopolar, bipolar, and fully-parallel designs. Tests on these three probe types have shown them to be functional at low voltage, but have also revealed several minor problems that must still be corrected as discussed in the last quarterly report. All of these problems can easily be corrected with the exception of the background supply current, which has been the subject of investigations during the past quarter. This background current, which can reach milliampere levels, does not affect probe operation but only adds a parallel current in the supply. Nevertheless, its origins must be understood and eliminated.

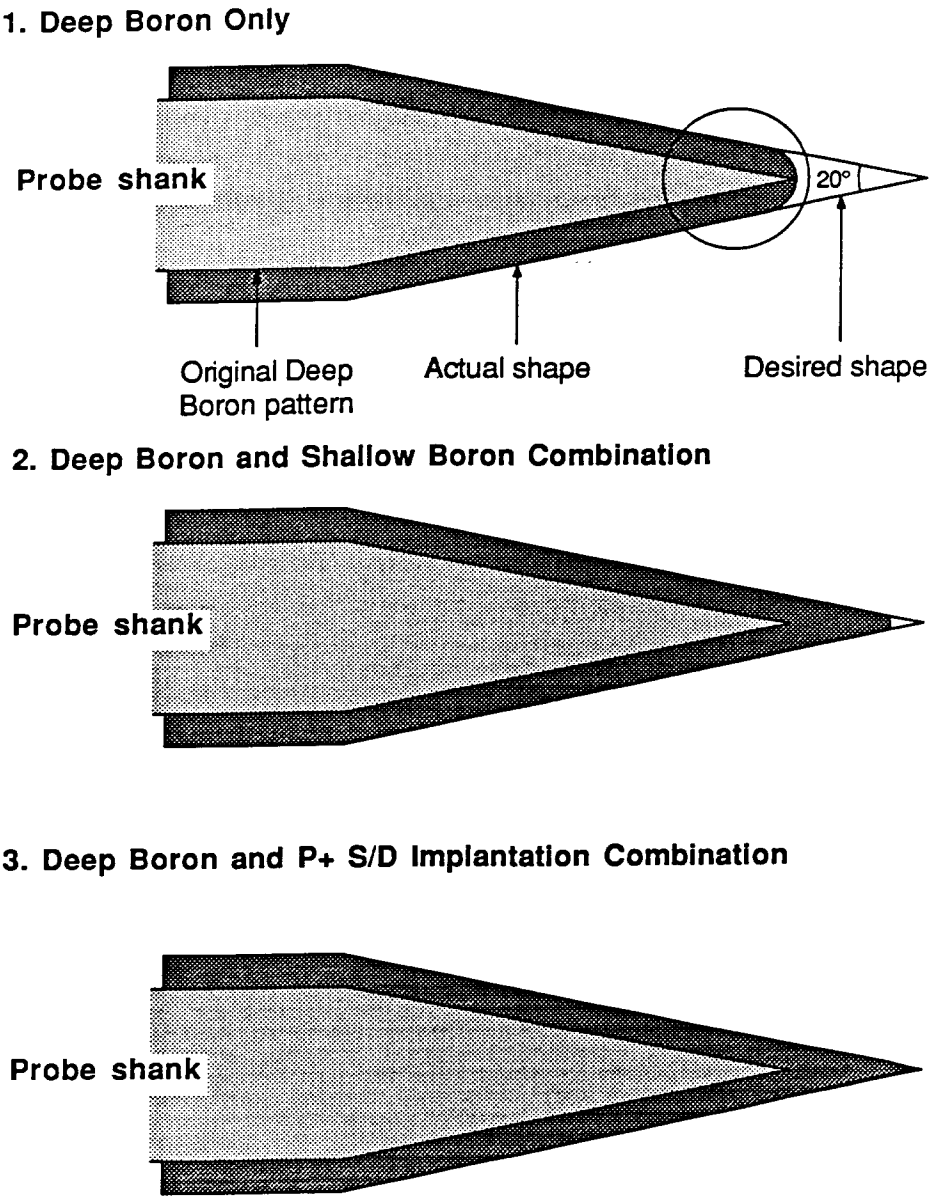


Fig. 2: Comparison of different diffusion techniques for forming sharp probe tips. Case 1 (top): deep diffusion only; case 2 (center): combined deep and shallow diffusion; case 3 (below): deep shank diffusion with shallow ion implantation of boron at the tip.

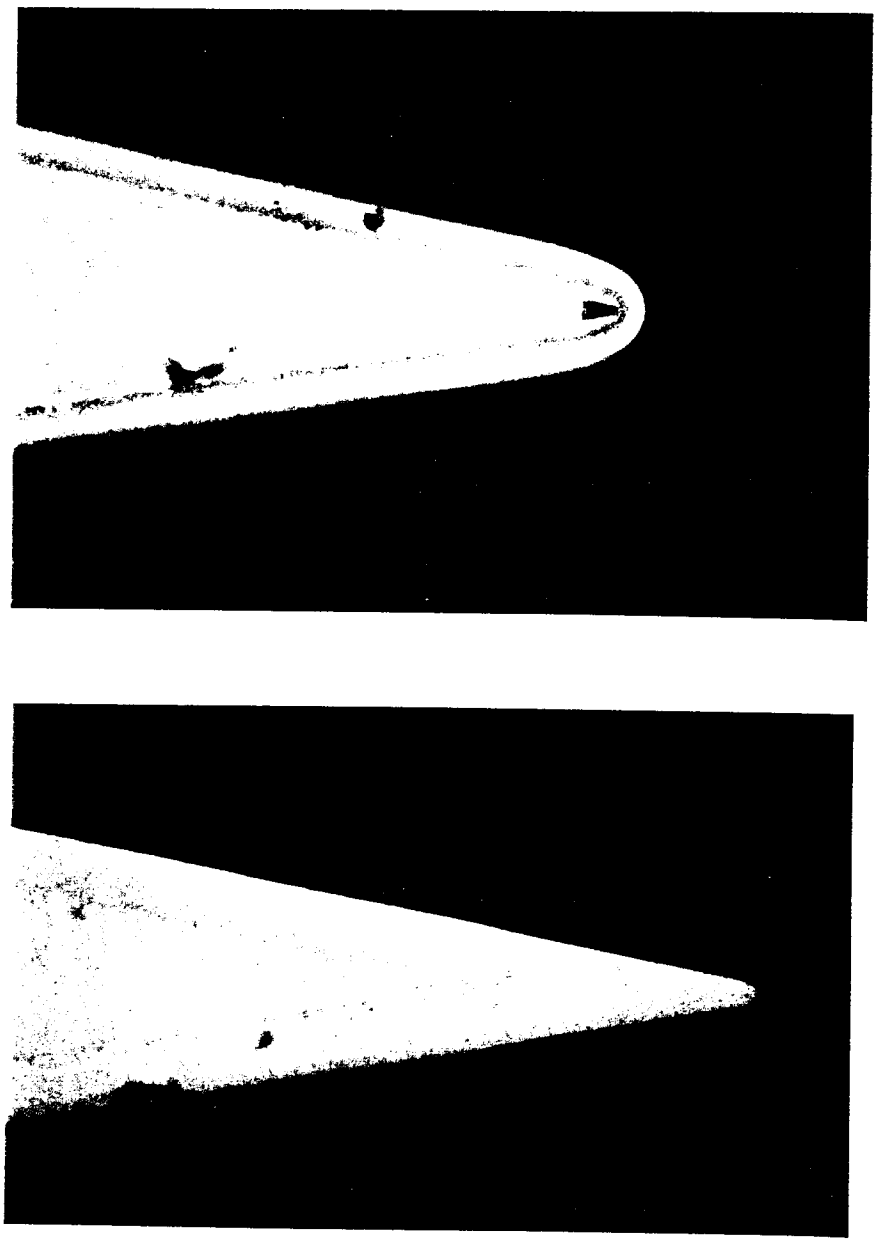


Fig. 3: Photographs of probe tips fabricated by deep boron diffusion only (top) and a combination of a deep diffused shank with a shallow diffused tip (below).

We have also sent had the circuitry for STIM-2 fabricated at the MOSIS foundry during the past term and have tested the circuitry to verify its operation for a series of second-generation probes. These test results are also presented in this section.

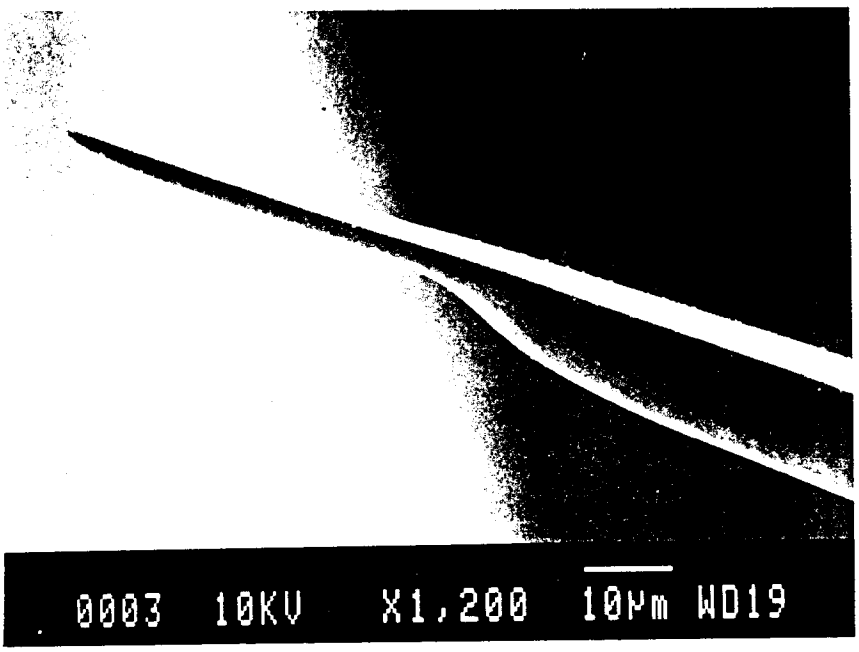


Fig. 4: SEM view of the thickness of a probe fabricated using a shallow boron diffusion for the tip combined with a deep-diffused shank.

4.1 Fine-Tuning the STIM-1 Design

a. Punch-through Voltage

As discussed in the previous report, tests on the STIM-1 probes have shown them to be functional at low voltage but at higher voltages there is an excessive background current that appears and is strongly voltage dependent. This appears to be due to either punch-through between the p-wells and the substrate across the relatively thin n-epi layer (~10 µm) or perhaps due to the turn-on of parasitic bipolar transistors which are inherent in the structure. Even using the modified micromachined CMOS process implemented with two-step deep boron diffusion process, further process optimization still seems to be needed. During the past quarter, we have studied three possible paths by which this current could be generated in an effort to understand (and eliminate) its source: 1) vertical punch-through, 2) lateral parasitic device operations, and 3) latch-up problems. The results in each of these areas are discussed below.

Punch-through occurs when the depletion regions from two reverse-biased p-n junctions extend completely across the intervening region between them so that they touch, allowing high current to flow between them. In order to evaluate punch-through as a

problem in our device structure, especially between the p-wells and the p-substrate, measurements have been performed on three different variations of our basic device structure: 1) the original CMOS process (single-step deep boron diffusion) having an n-epi thickness of 10 μm, 2) a modified CMOS process (two-step deep boron diffusion) with an n-epi thickness of 10 μm, and 3) the original CMOS process with an n-epi thickness of 16 μm. Figure 5 shows electrical test results performed to test the punchthrough voltage between the p-well and the p-substrate. As can be seen in this graph, the modified CMOS process (2nd run of STIM-1) is significantly better than the original CMOS process (1st run of STIM-1). In the first CMOS run, the p-wells were essentially shorted to the substrate so that at 2V VDD, a substrate current of 20 mA is generated. For the modified process and a 10μm epi thickness (but a shallower p-well), the leakage is 0.44mA at 5V. This is still too large, but at least much better than before. For the original CMOS process with thicker epi material (16μm), punchthrough is essentially eliminated as a problem, with a current of only 0.04μA at 5V. Based on these measurements, we plan to use a thicker (16μm) epitaxial thickness for all future fabrication of the active stimulating probes. Figure 6 shows the p-well doping profile and the deep-boron-diffusion profile for the resulting process. The etch-stop depth is about 13μm for the probe shank with a p-well junction depth of about 4.5μm.

b. Lateral Parasitic Device Operation

A second potential source of spurious leakage current is the turn-on of parasitic lateral bipolar devices in the structure (e.g., lateral p-n-ps between adjacent p-wells or between p-wells and the ground diffusion). In order to test this as a source of background current, we selected a small circuit block (DAC and counter) which has the same design for all of these different process options. The selection of this small circuit block eliminates any complicated circuit design problems so that the results only represent process related problems. Measurements have been performed for three different cases: a) the MOSIS CMOS process (no p-substrate and a shallow p-well diffusion); b) the original CMOS process (no p-substrate and a deep p-well diffusion); and c) the modified CMOS process (p-substrate and a medium p-well diffusion depth) with the n-epi thickness of 10 μm. To eliminate vertical punch-through effects, all pads were connected to ground except the Vss pad (p-well), and the Vcc pad (n-epi) was swept from 0V to 20V with Vss varied as shown (from right to left: 0V, -5V, and -10V for each group). This test results will represent any lateral parasitic device operation such as lateral punch-through or parasitic BJT operation.

Figure 7 compares the electrical test results for the three different cases. As can be seen in this graph, case (b) shows the largest background for a given Vcc, reaching 8mA at 5V. This may indicate that the deep diffusions punched laterally through to the p-wells. In case (c), even though this structure has a parasitic vertical pnp BJT structure (p-well, n-epi, and p-substrate), the current level is still much lower than that of case (b). This indicates that a shallow p-well diffusion might be very helpful in reducing the stand-by current. However, the current is still too high at about 2mA at Vcc = 5V. In case (c), however, it is not clear that all vertical problems are being suppressed. More tests will be done to clarify the performance in this case. Finally, in case (a) the lateral conduction is satisfactory, with the current less than 0.1mA at 5V and still still less than 1mA at 15V. In this case there is no p-substrate (so vertical parasitic devices and punchthrough do not exist) and the p-wells are shallow, reducing lateral effects. This result indicates that if we are careful with regard to junction depths, the process and device structures we are using will perform adequately.

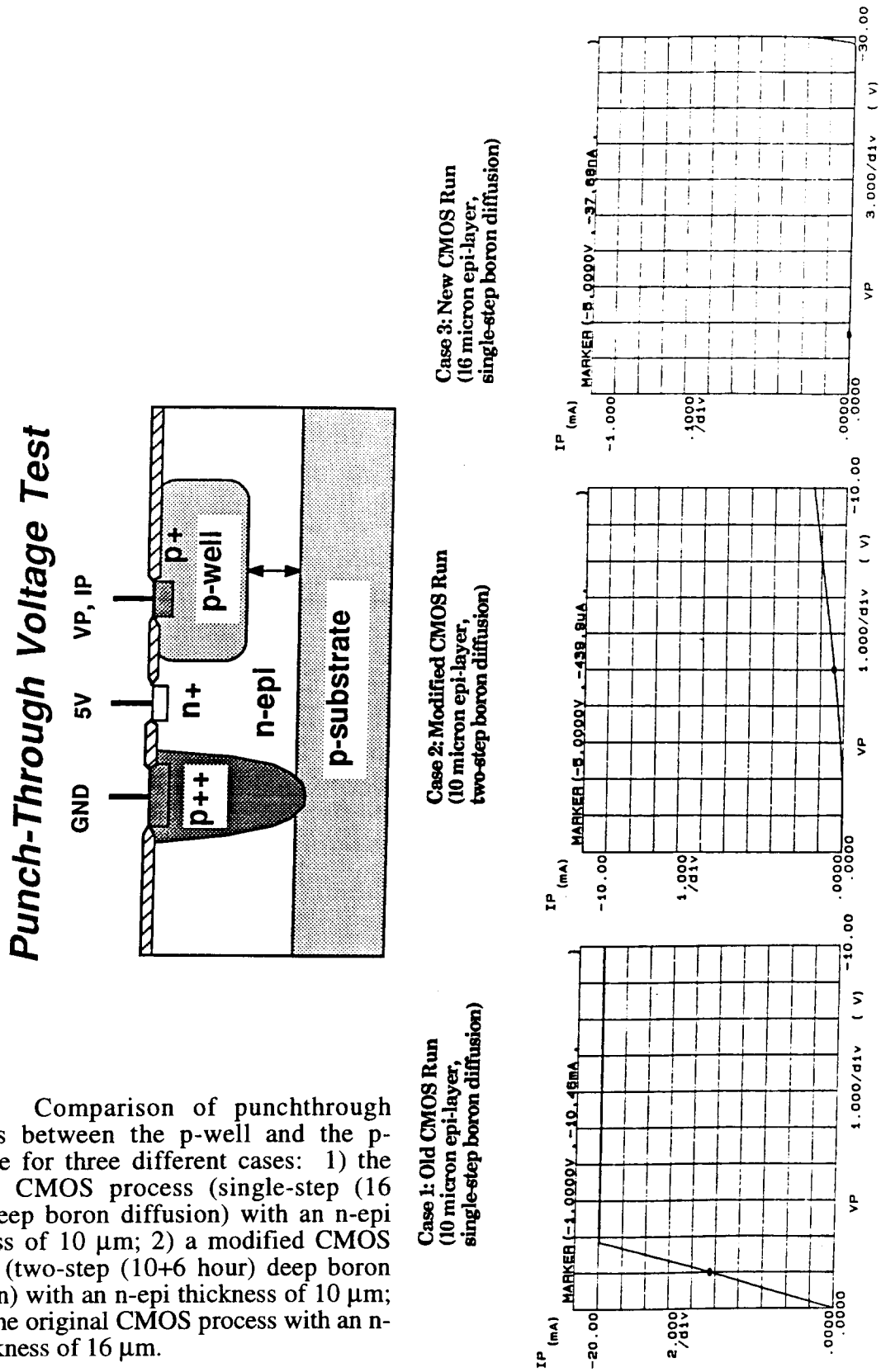


Fig. 5: Comparison of punchthrough voltages between the p-well and the p-substrate for three different cases: 1) the original CMOS process (single-step (16 hour) deep boron diffusion) with an n-epi thickness of 10 μm; 2) a modified CMOS process (two-step (10+6 hour) deep boron diffusion) with an n-epi thickness of 10 μm; and 3) the original CMOS process with an n-epi thickness of 16 μm.

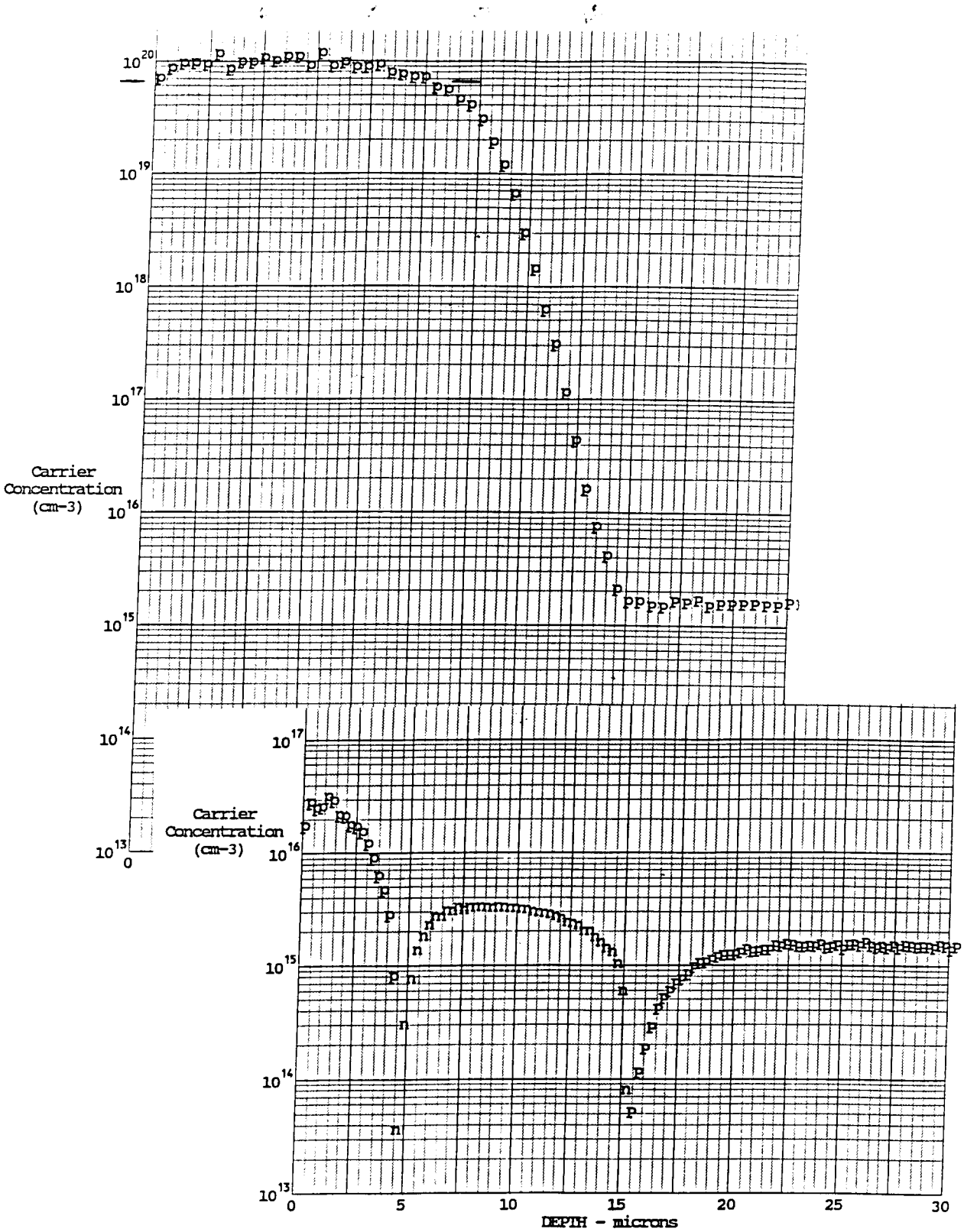


Fig. 6: Measurement results of the doping profiles in the case of a modified CMOS process with an n-epi thickness of 16 µm: below: p-well to p-substrate doping; and above: deep boron diffusion profile.

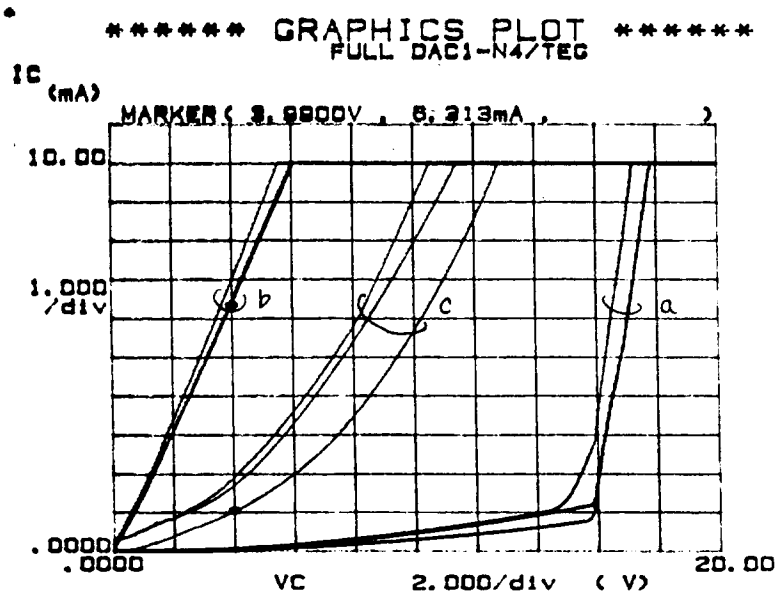


Fig. 7: Comparison of electrical test results according to three different cases; (a) MOSIS CMOS process (no p-substrate and shallow p-well diffusion), (b) old CMOS process (no p-substrate and deep p-well diffusion), (c) modified CMOS process (p-substrate and medium p-well diffusion) with the n-epi thickness of 10 μm. To eliminate the vertical punch-through effect, all pads are connected to ground except Vss pad and Vcc pad is swept 0V to 20V with the variation of Vss voltage (from right to left 0V, -5V, and -10V for each group).

c. DC Latch-up test for STIM-1 Probes

All CMOS integrated circuits have a latch-up problem due to the parasitic devices inherently hidden in the device structure. We performed DC latch-up tests for STIM-1 probes at both the wafer and chip levels to see how immune they are to this problem (the AC latch-up test is a more severe test because it includes transient noise possibilities during clocking). The conditions of this test were as follows: all pads were connected to ground and a positive current was forced into the Vcc pad until the Vcc voltage limited at given compliance level (10 or 20 V in this test). As can be seen in Fig. 8, the current levels as a function of Vcc are excessive for both STIM-1 and -1a, although it is not clear that this current is a true latch-up current. Rather, we believe we are seeing another manifestation of the lateral and vertical current problems of the previous sections. In the case of wafer-level measurements on STIM-1b, the situation is better, perhaps because the substrate is thicker and minimizes parasitic resistance drops there.

In examining these results, it is clear that the first run of STIM-1 probes resulted in punch-through between the p-wells and the substrate. It is also evident that there are lateral punch-through problems or (alternatively) problems with parasitic lateral bipolar devices in

the cases where a deep p-well is used with a shallow (10μm) epi thickness. However, when the p-well is kept relatively shallow and the epi is thick (16μm), the vertical and lateral leakage levels are at acceptable levels. It is also obviously important to provide frequent ground contacts to the substrate and isolation (deep-boron) diffusions as well as frequent contacts to Vcc for the epi islands in order to avoid parasitic resistance drops that can allow parasitic bipolar devices to turn on. All of our probes are now being run on 16μm epi material. It is noted that these problems are much less of a problem in the recording probes since they do not require a negative supply and therefore do not have an active substrate pnp transistor present.

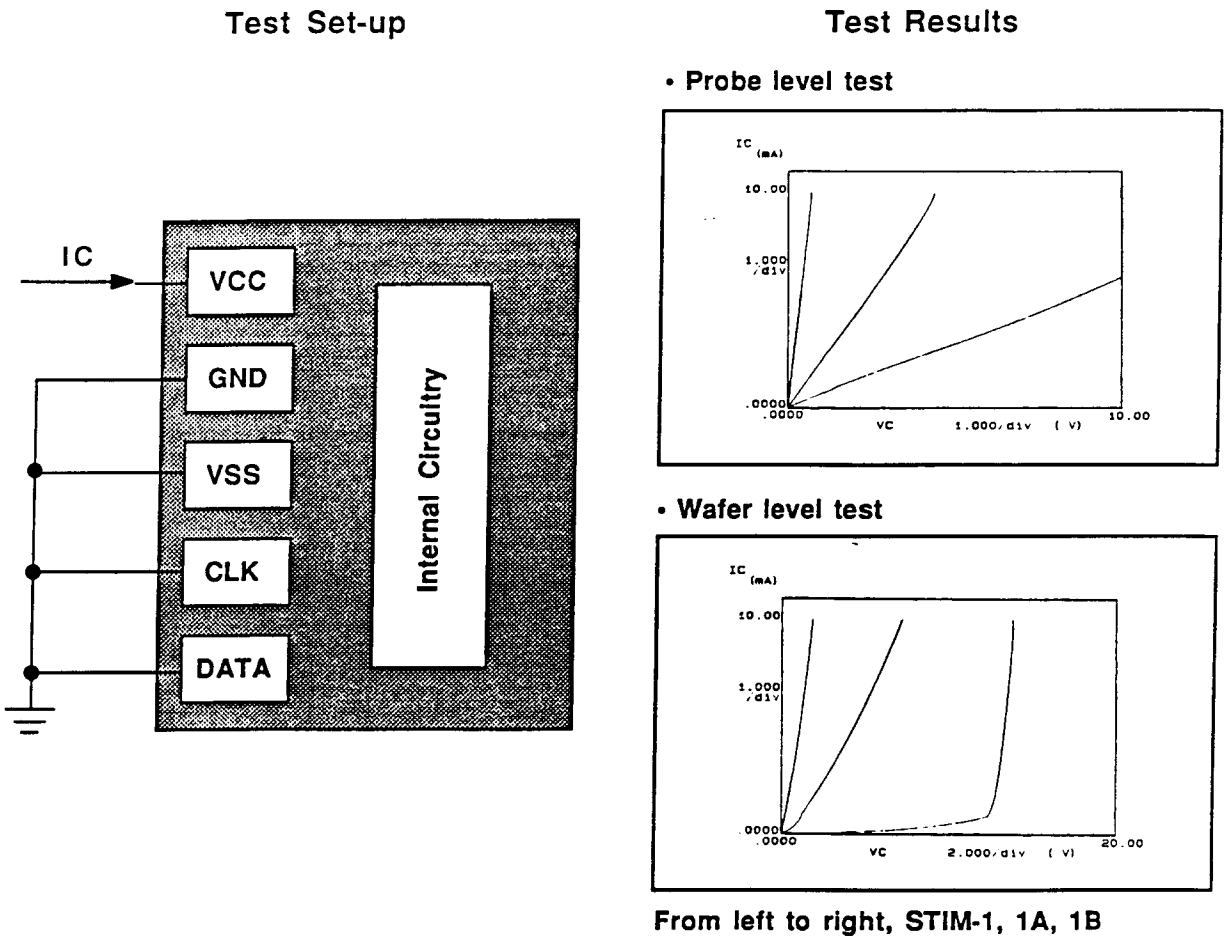


Fig. 8: DC latch-up voltage test results on actual probes: (a) wafer level and (b) probe level. In these graphs, the curves correspond to STIM-1, STIM-1A, and STIM-1B from left to right.

4.2 Test Results on the Circuitry for a Second-Generation Active Probe: STIM-2

During the past quarter, we completed the design of circuitry for a second-generation active probe and had the circuitry integrated using the MOSIS foundry service. The design features of this circuitry were discussed in the previous quarterly report. The test results for this circuitry will be presented in this section. The results are very encouraging with almost everything working as designed. MOSIS ran the STIM-2 chip through the Orbit foundry, whose process characteristics are close to ours in most cases and yet are somewhat different in a few paramters. Below is a comparison of a few of the SPICE model parameters between our design targets and the MOSIS/Orbit process.

Table 1. Comparison of transistor design characteristics and the actual MOSIS values.

SPICE Parameters	n-MOS		p-MOS	
	Design	MOSIS	Design	MOSIS
VTO (V)	0.7	0.9018	-0.7	-0.7183
KP ($\mu A/V^2$)	70	52.096	55	20.177
Tox (Å)	300	427	300	427
ΔL (μm)	0.0	0.637	0.0	0.33
ΔW (μm)	0.0	0.089	0.0	0.947
LD (μm)	0.2	0.2789	0.4	0.1585
GAMMA ($\sqrt{V}$)	0.98	0.9374	0.07	0.4698
LAMBDA (1/V)	0.025	0.02169	0.09	0.03506

As can be seen above in Table 1, the actual current driving capability of the MOSIS CMOS devices is much lower than that of design, which results in lower output current magnitude from the DAC and slower speed. Fortunately, most of the circuitry in the STIM-2 circuits exhibits digital operation and was designed with enough latitude to handle these parameter shifts without adverse effects on functionality. The DAC current shifts can be easily compensated by adjusting the positive and negative supply voltages.

Testing of the MOSIS circuit consisted of two basic parts. First, the simple test blocks included on the MOSIS chip were evaluated. Next, the STIM circuits themselves were examined.

Simple Test Blocks

For improved functionality, this second-generation active stimulating probe has been designed carefully and efficiently. The new probe contains a number of newly designed circuits and other features, including a negative pulse detector, a clock-controlled decoder with fewer transistors, a simple level-shifter having no static power dissipation, wider lateral clearances around the p-well to ensure freedom from lateral punch-through, and the use of wider metal for the power buses. The next sections describe the important primary circuits designed for this probe. Using these circuits, a high performance active stimulating probe can be achieved.

The following are the results of the test blocks that were evaluated. These are test devices or circuits that are included on the chip for individual evaluation. These circuits

were tested before the full STIM-2 circuits in an attempt to locate potential problems and be able to deal with them while testing the full STIM-2 circuits.

A. Low Power Digital-to-Analog Converter (DAC) Current Source

The stimulating electrode sites are driven by an 8-bit CMOS DAC as shown in Fig. 9. It is controlled by a seven-bit channel latch which controls a string of current mirrors. To effectively stimulate the tissue, a bipolar current driving scheme was adopted; both current sourcing and sinking operations are possible on the sites during the active stimulating cycle. This concept, which is based on charge balance, efficiently stimulates the tissue while reducing tissue damage and improving probe reliability. The DACD (DAC disable) and CP (current polarity) clocks control the overall DAC operation. The DACD clock is generated in the recording and platform address modes to disable the DAC. During the normal active cycle, the CP clock selects either p-DAC (CP=1) or n-DAC (CP=0), and a total reference current of only 1μA flows for the control of a whole string of current mirrors, resulting in a small layout area and low power consumption. The current levels of the other transistors are designed to double at each successive stage using the same unit transistor, resulting in high current linearity regardless of power supply voltages and process parameters. In the case of sourcing (sinking) current, inputs D0 through D6 for the DAC turn on their corresponding p-MOS (n-MOS) switches when at Vss (Vcc) and then turn them off when at Vcc (Vss). A level-shifter interfaces standard CMOS voltage levels (GND to Vcc) to the inputs of the DAC (Vss to Vcc). This power-efficient DAC is designed to deliver bipolar current ranging from -127 μA to 127 μA with 1 μA resolution.

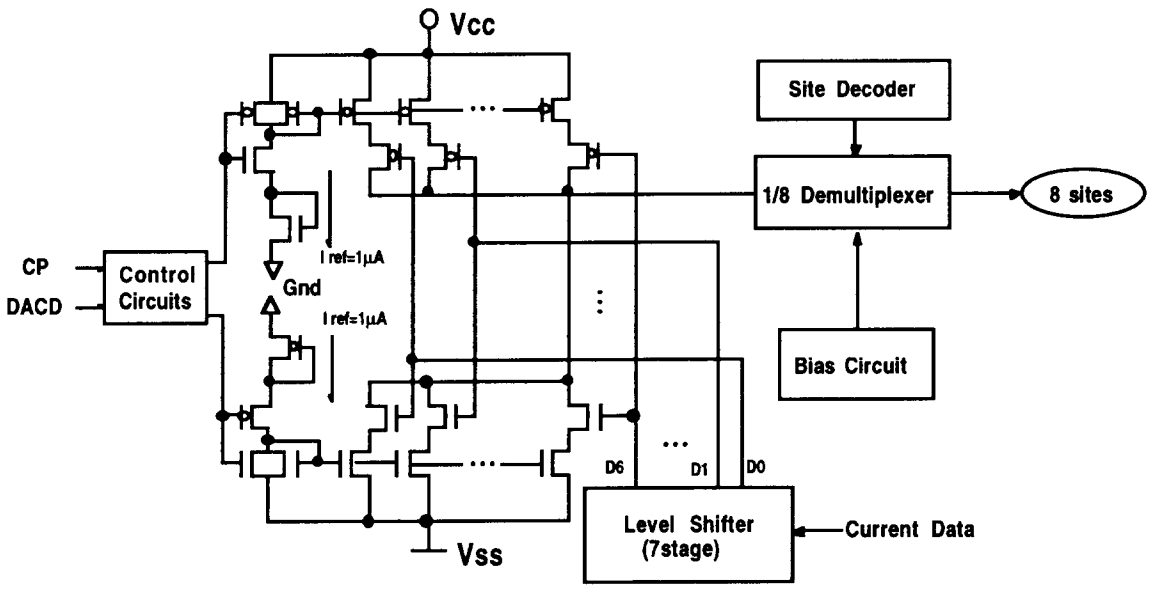
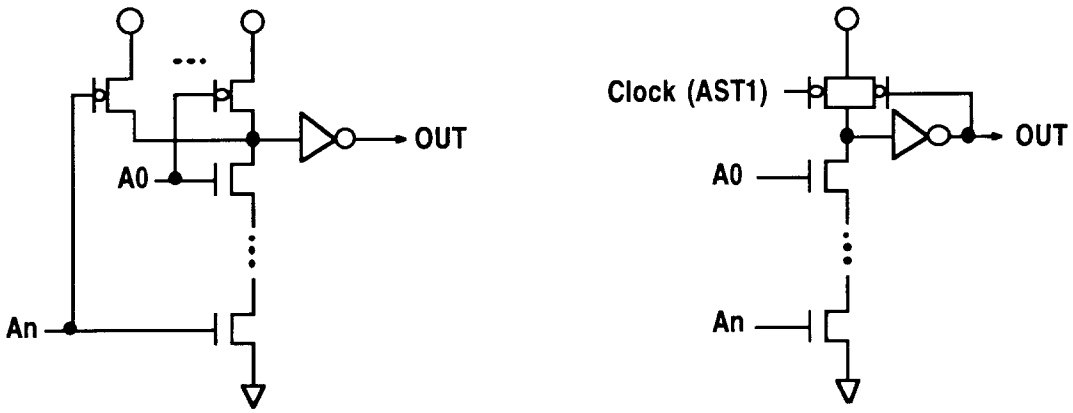


Fig. 9: The low-power digital-to-analog converter (DAC) current source circuit.

B. Clock-controlled Address Decoder

The decoder is needed to select one of eight DACs or a specific site out of eight electrodes. As the number of address inputs is increased, the gate loading capacitance must seriously be considered to ensure high-speed circuit operation and low power

consumption. This clock-controlled scheme can reduce both propagation delay time and layout area by half compared with the conventional NAND-type decoder in the case of having many input signals because there is no need for extra p-MOS load transistors. Figure 10 shows the circuit diagram of the conventional NAND-type decoder and the newly designed clock-controlled decoder. As can be seen in this graph, the clock-controlled decoder scheme is very useful as the number of input address bits increases.



(a) Conventional NAND-type decoder

(b) Clock-controlled decoder

Fig. 10: Circuit diagram of a conventional NAND type decoder and the newly designed clock-controlled address decoder.

C. Operational Amplifier for Electrode Recording

Figure 11 shows the circuit configuration of a band-pass operational amplifier to record the neuronal signals. The performance of the amplifier plays a dominant role in the accurate reproduction of these signals. In this design, a simple and efficient amplifier was adopted in order to achieve reliable circuit operation in terms of bandwidth and process insensitivity. The neural signals have frequency components of interest from 100Hz to about 10kHz. In the amplifier designed for this neural probe, low-frequency feedback is used to reduce the amplification of DC signals and allow the use of higher amplification factors for the lower-amplitude neural signals. The very low cut-off frequency required for DC gain reduction is realized by using a diode-capacitor filter as in PIA-2. This configuration is simple and takes only a small amount of chip area. Figure 12 shows a test result for this operational amplifier. The upper trace is a sine wave input and the lower trace is the output voltage with a gain of 28.

D. Simple Level-Shifter having No Static Power Dissipation

The level-shifter converts standard CMOS input signals (Vcc (H) to GND (L)) to appropriate inputs for the DAC (Vcc (H) to Vss (L)). A minimum of 7 level-shifters is needed for each DAC so it must be designed to minimize the static power consumption and layout area. This novel circuit needs only six transistors to meet the above requirements by using a feedback control scheme. The feedback control scheme returns the output signal to the input circuitry in order to avoid static power dissipation. High switching speed (a simulated propagation time of less than 5nsec for C_{load}=0.3 pF) can be achieved using

small transistors. A circuit schematic and test results for this circuit block are shown in Fig. 13.

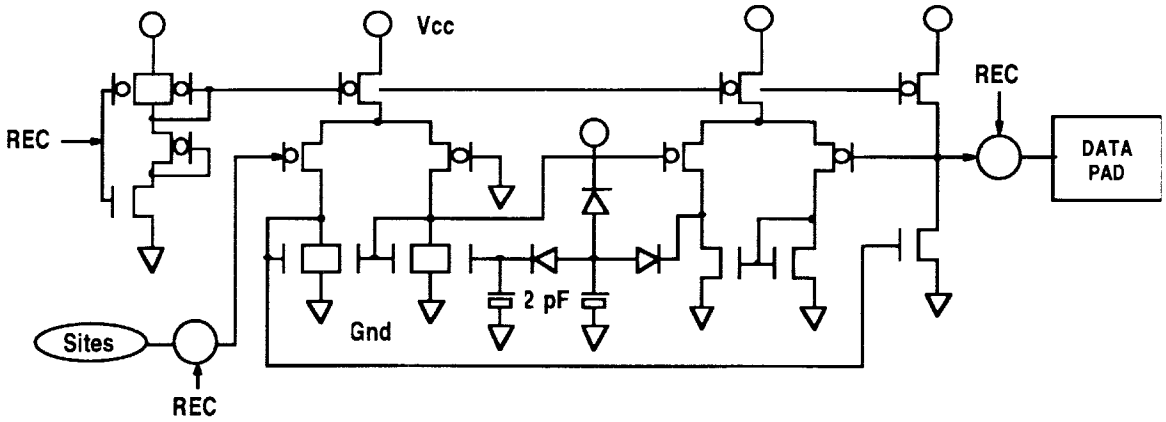


Fig. 11: Band-pass operational amplifier for neural signal recording.

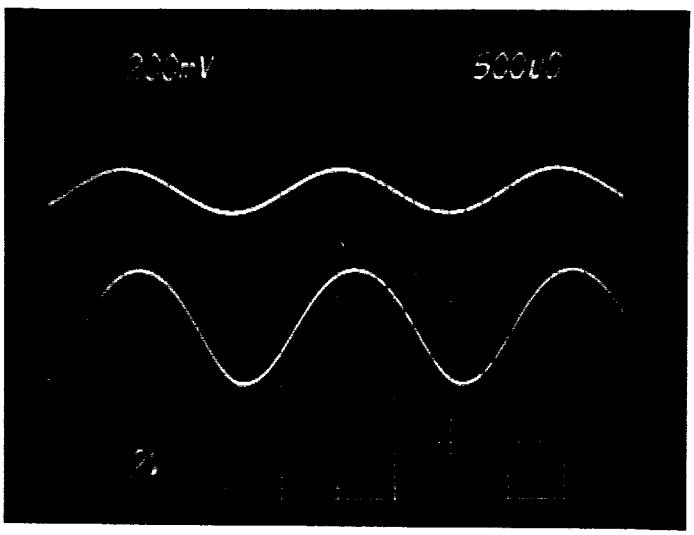
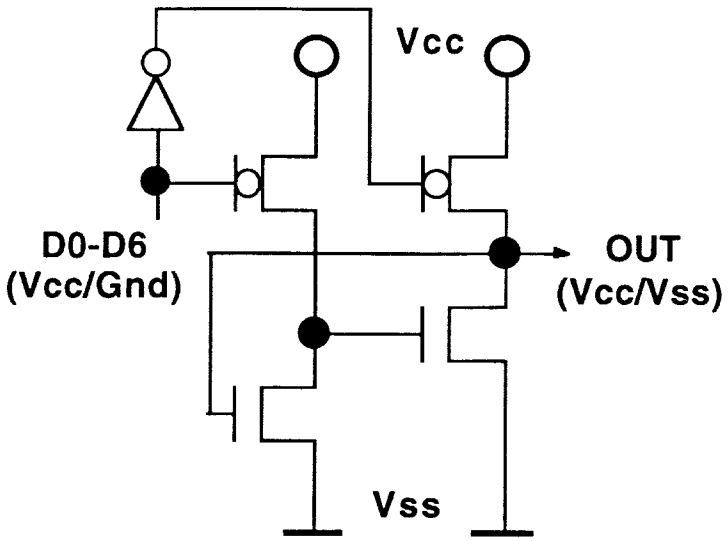


Fig. 12: Test results for the operational amplifier.

E. Power-On-Reset (POR) Clock

Figure 14 shows the circuit diagram of the power-on-reset (POR) clock which is used for activating sites before stimulation and for precharging the overall circuitry to the correct initial conditions. The POR signal is generated by the application of the positive power supply, Vcc, and goes to ground when the first clock arrives. It stays in low during operating cycles due to the latching-type of circuit configuration used.



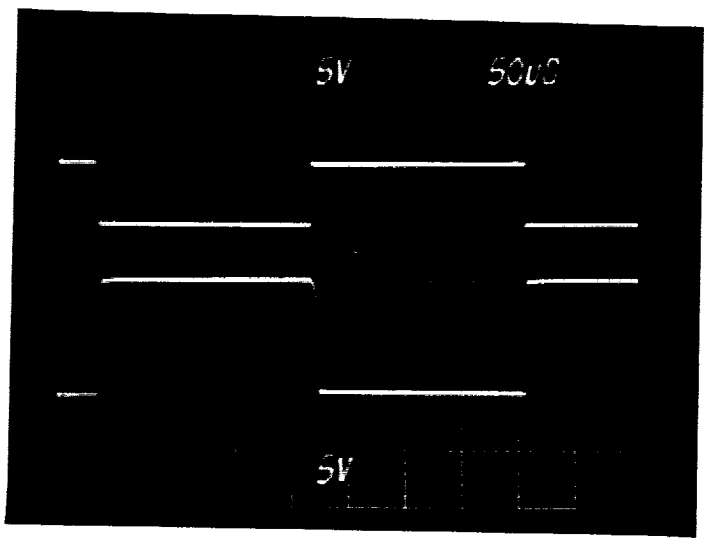


Fig. 13: Circuit diagram of a level-shifter with no static power dissipation and the measured test results from this circuit block.

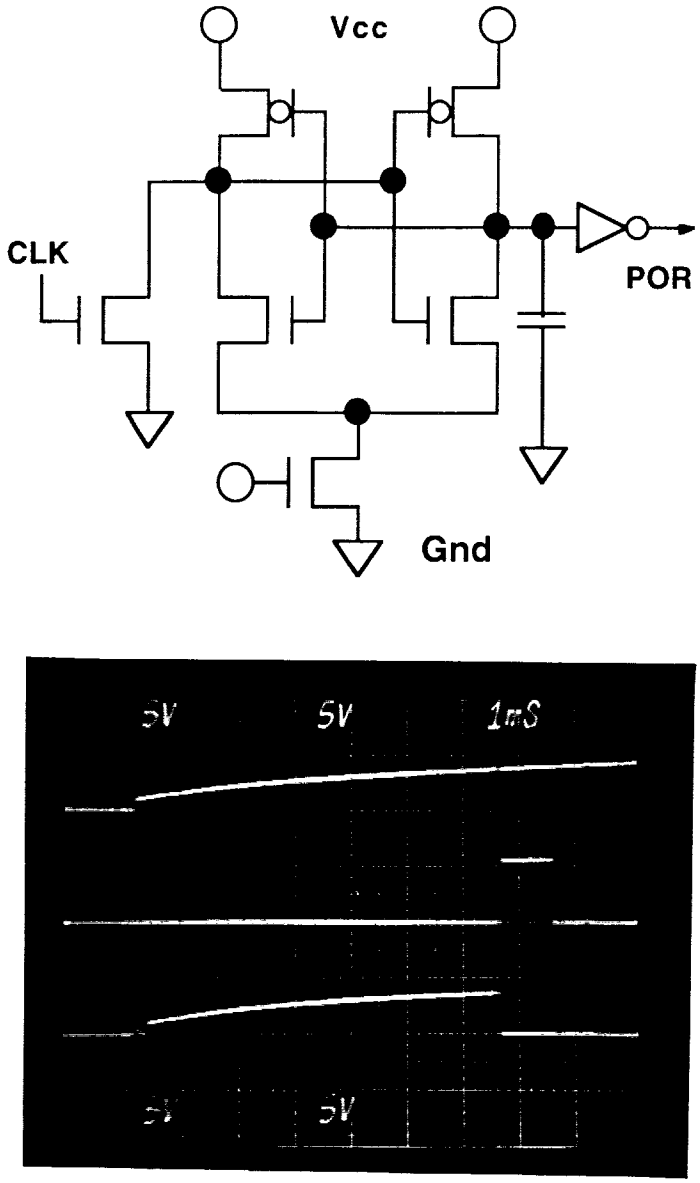
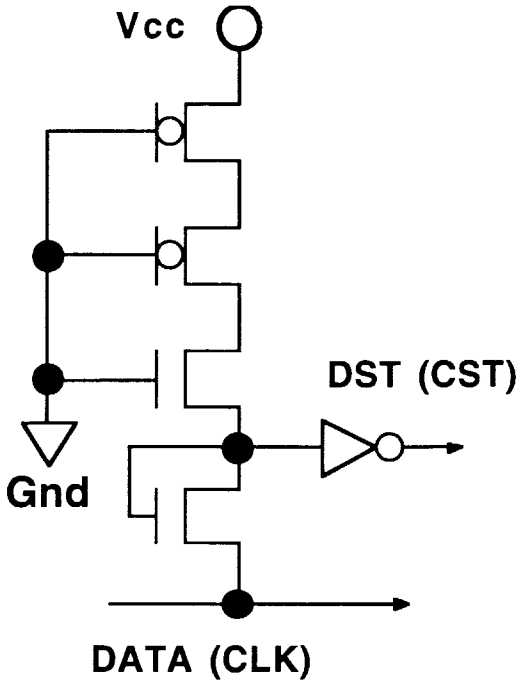


Fig. 14: Circuit diagram of the power-on-reset clock circuit and its test results.

F. Negative Pulse Detector (for CST and DST clocks)

In order to effectively synchronize the stimulating probe with the external control system, the use of the negative power supply level (Vss) may be a option from which to generate the clock because most of the CMOS circuits use Vcc and GND levels only. Figure 15 shows a negative pulse detector in this design, for the CST (CLOCK strobe) or DST (DATA strobe) clocks, to initiate latching of the address, mode, and current data bits provided by the external CLOCK and DATA signals. This circuit scheme is specially designed for a small layout area and low power consumption. If the input level of the control signals (CLOCK and DATA) are either Vcc or GND for normal data transfers, then

the CST (DST) clock stays at ground (L) with no static power consumption. When the input levels are negative (Vss), this clock goes to the high state (Vcc) and remains there until the negative input pulse disappears, so that it can generate pulses according to these input signals when synchronizing pulses are needed.



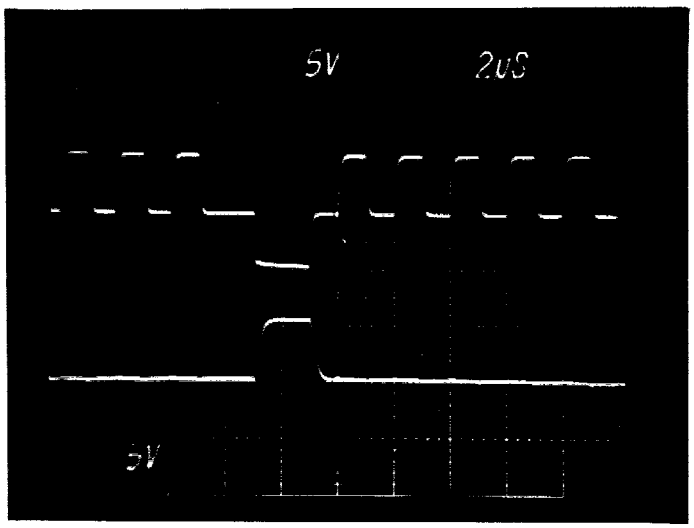


Fig. 15: Circuit diagram of the negative pulse detector and the measured test results.

STIM Circuits

The MOSIS chip is packed in a 64 pin PGA (Pin-Grid-Array) package. This chip is inserted into a ZIF (Zero-insertion-force) socket which is mounted on a customized circuit board which is designed to reduce line impedance for high circuit performance. Using an HP 8016 word generator, serial clock and data inputs can be generated with limited commands (a maximum of 2 commands) since 18 actual clock cycles are needed for the STIM-2 circuits instead of 16 clock cycles for STIM-1. These inputs are converted into actual clock and data signals (tri-level) for STIM-2 by customized tri-state buffers. The operating frequency for the clock and data inputs can be adjusted using word generator frequency setting. *The test results show that all of the probe circuits operate as designed.* The table below shows the specifications for the final STIM-2 probe.

Table 2: Specifications for the second-generation stimulating probe, STIM-2

Process technology	3μm, p-substrate, n-epi, p-well single poly, double metal micromachined CMOS technology
Power supply voltage	Vcc = 5 V, Vss = -5 V, GND = 0 V
Control signals	DATA and CLOCK
Current range	-127 to +127 μA
Current resolution	1 μA
Power dissipation	Standby ≤50 μW, Operating ≤10mW
Operating clock frequency	4.5MHz (~222 nsec)
Time delay to select any site	4 μsec
Total external pads	5 pads (3 power, DATA, and CLOCK)
Electrode size	1000μm^2
Maximum shank width	99μm
Total stimulating sites	64
Chip area excluding shanks	11.29mm^2
Circuit features	• low-impedance shunt mode for idling sites • anodic bias mode for standby sites • electrode-impedance monitoring mode • electrode recording mode • self-test and trouble flag mode • electrode-activation mode • simple level-shifter with no static power • clock-controlled address decoder • low power current source (DAC)

Figure 16 shows a photomicrograph of the circuit portion of the active probe fabricated through MOSIS.

The following are the items measured thus far in the actual STIM circuits.

• The POR signal comes up in the correct state when the Vcc supply voltage is turned on. In this state, the sites are connected to the data pad for analog access to the sites during activation. The first positive clock pulse resets the POR circuit correctly. Figure 17 shows the presence of an analog connection from data pad to sites. An arbitrary data waveform is applied and measured at site #10 when Vcc power is on and no clock has yet been received.

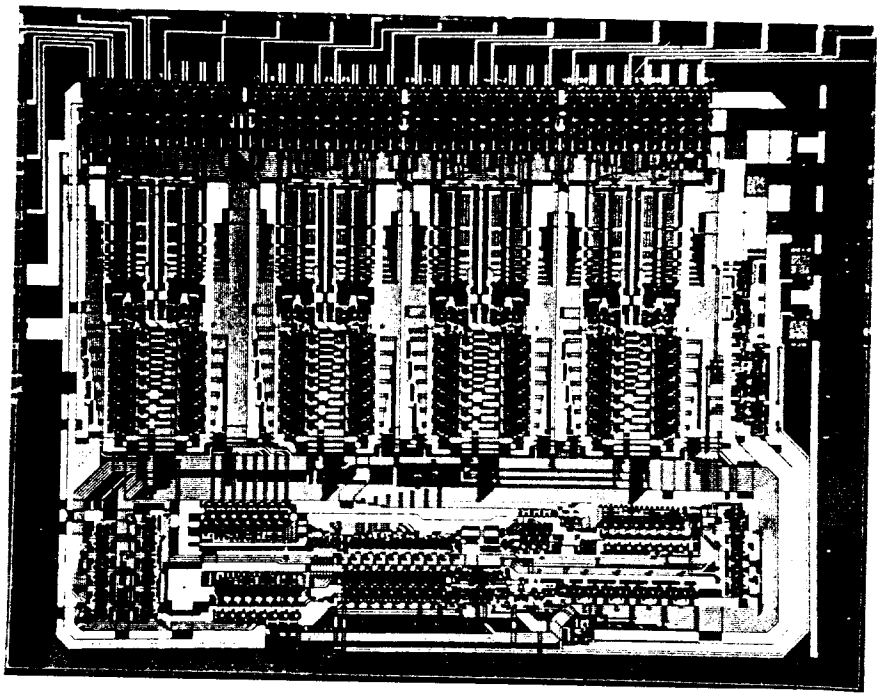


Fig. 16: Photomicrograph of the circuit portion of the active STIM-2 probe fabricated through MOSIS.

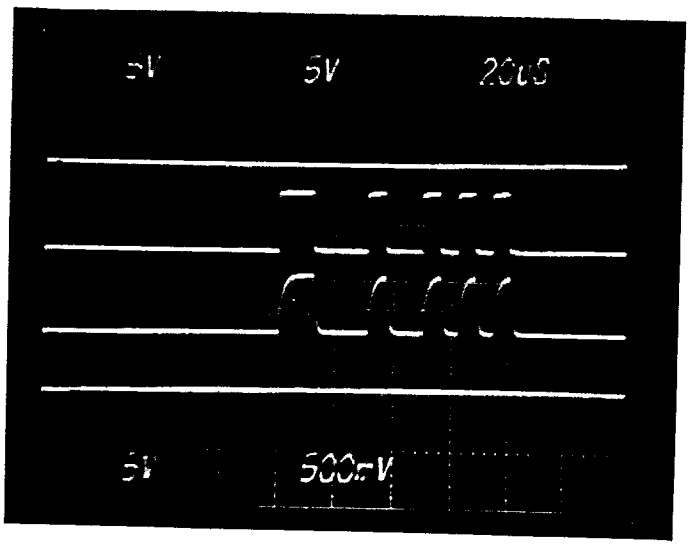


Fig. 17: Analog connection from data pad to sites when Vcc power is turned on and no clock has been received. Vcc = 5V. The traces are (top to bottom) clock, data, site #10, and POR (high).

• The input shift register accepts data serially with the clock. Figure 18 shows the output of the shift resister during clocking. In this case, output 0 (000) and output 7 (111) are selected.

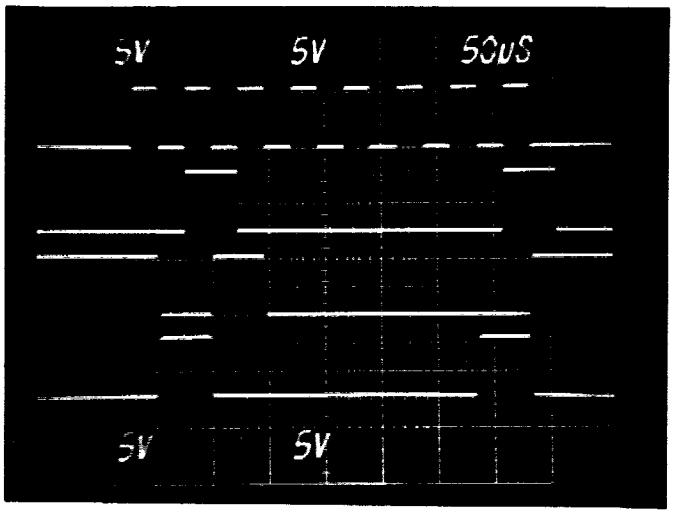


Fig. 18: Output of the shift register during clocking. In this test, output 0 and output 7 are selected. The traces (top to bottom) are clock, data, SH0 (1), and SH7 (8).

• The address and mode latches at the output of the shift-register latch onto the data when strobed by a negative pulse on the data line (DST clock), and the address and mode decoders properly decode the address and mode states and enable the appropriate channel. Figure 19 shows an address decoder output of DEC24 (DAC decoder for #4 (100)), alternating two different addresses. During the falling edge of the DST clock, the actual address is latched. In this test, DAC4 is selected.

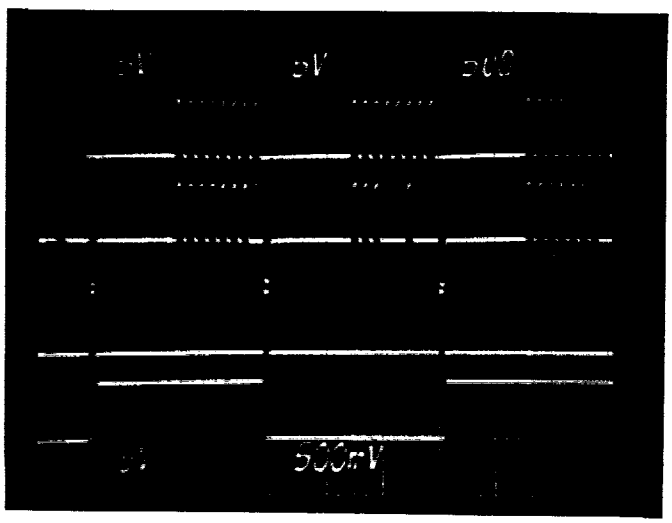


Fig. 19: Address decoder output of DEC24 (DAC decoder for #4 (100)), alternating two different addresses. The traces are (top to bottom): clock, data, strobe, and DEC24 out.

• The addressed per-channel data latches lock onto the data when the clock line is strobed negatively, and the DACs generate the appropriate currents. Figure 20 shows output voltage waveforms across a 5.5KΩ resistor load when the current level data are alternating from (0111111) to (1111111) for sourcing (CP=1) and sinking (CP=0) cases, respectively. Figure 21 shows circuit operation (current waveforms on site 1, alternating between full-scale sourcing and full-scale sinking across a 5.5 kΩ resistor).

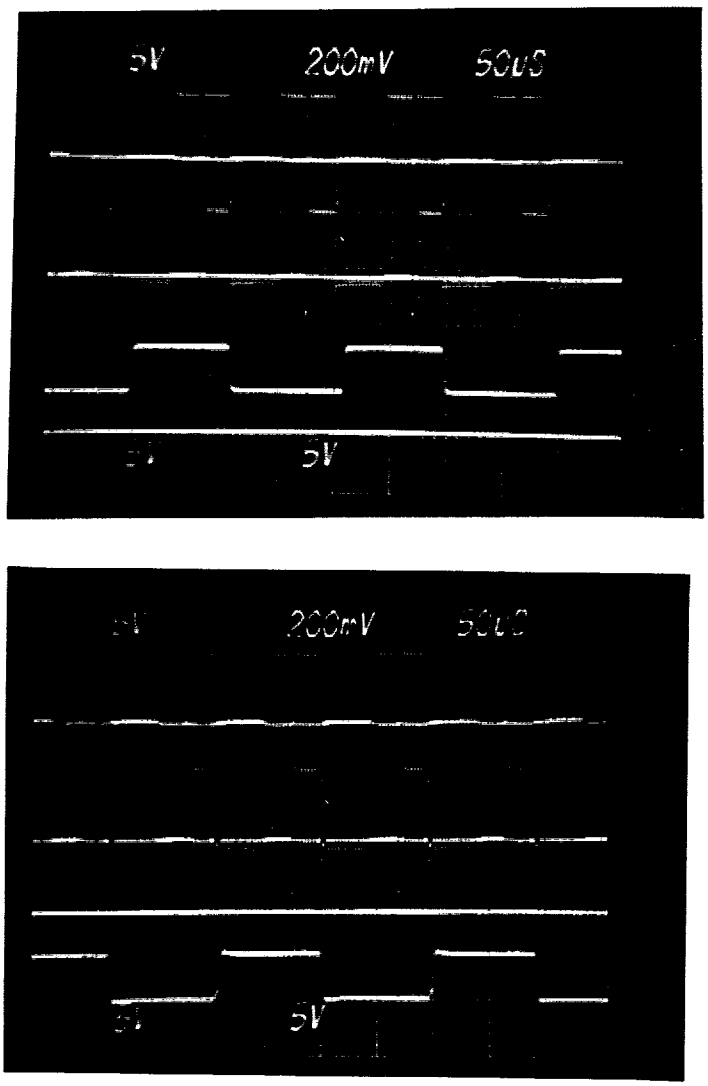


Fig. 20: Output voltage waveforms across a 5.5KΩ resistor load when the current level data are alternating from (0111111) to (1111111) for sourcing (CP=1, above) and sinking (CP=0, below) cases, respectively. The site output is shown on the third trace from the top in the upper photo and the fourth trace from the top in the lower photo, with the first two traces showing the clock and data. The fourth and third traces, respectively, provide a ground reference.

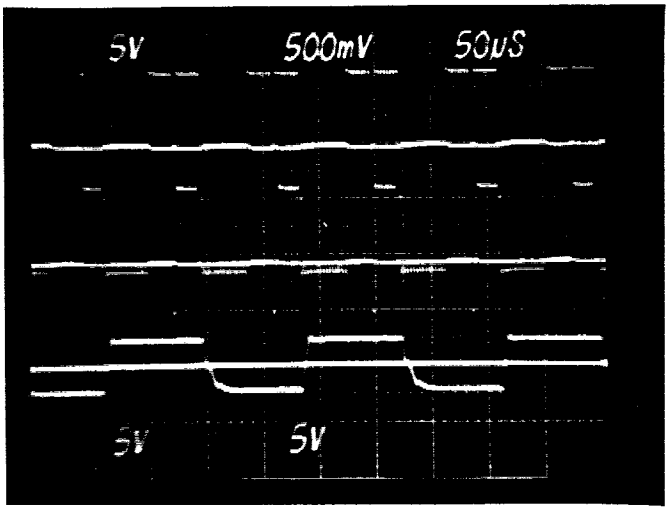


Fig. 21: Circuit operation: current waveforms on site 1, alternating between full-scale sourcing and full-scale sinking across a 5.5 kΩ resistor. The ground reference is superimposed on the output current swing.

The correct operation of the full circuitry for STIM-2 is very encouraging. We are proceeding to lay out a new set of probes for STIM-2 and expect to fabricate them in late summer or early fall. Prior to that, we intend to more fully understand the background current present on STIM-1 so that we are sure to avoid it on STIM-2 and so that STIM-1 can be rerun in order to obtain working probes of those designs as well.

5. STIM 2 External Interface Electronics

During the last quarter, some cleanup work on the STIM-1/1a external electronics was done in preparation for the STIM-2 enhancements. Work was also started on the STIM-2 enhancements themselves. The implementation is being done as an enhancement of the existing STIM-1/1a interface so that a single piece of equipment can be utilized for all three cases. There are several areas where changes are required to implement the STIM-2 communication protocol. Some changes to the Chimera DSP daughter board electronics are required. In the context of that work, a major redesign of the PAL logic on the daughter board which generates much of the timing is necessary. In connection with the daughter board changes, the software on the DSP board that services the daughter board, and the C program on the PC that communicates with the DSP board must be enhanced.

The cleanup work on the STIM-1/1a interface involved the elimination of a few bugs in the support software and bringing the documentation fully up to date. A bug in the single stepping control routines in the C program on the PC was eliminated. This had been causing twice as many steps as requested to occur due to an incorrect mapping from the state transition diagram for the daughter board hardware into control transitions. This feature now performs reliably. Problems in the word stepping software in the C program were also eliminated. The software was stepping by less than a whole word at a time.

This occurred because the software was not accounting for the wait states that are inserted by the daughter board hardware to stretch the data latching strobe to the probe. This was corrected and enhanced in anticipation of the STIM-2 requirements, where the number of single steps in a word would be different that for STIM-1/1a. The user can now specify word lengths over a wide range, which allows convenient execution of not only whole length words for testing but also of subunits like shifting and strobing in the site mode and address. The documentation cleanup brought all of the circuit diagrams fully up to date, as well as the comments in the C program.

The daughter board wiring enhancements for STIM-2 on the daughter board have been completed. These enhancements came in several areas. The control register definition had to be expanded to add a STIM-1/1a vs STIM-2 control bit. Accompanying wiring changes allowed the control register to communicate this information to the timing PAL. Another change allows the timing PAL to override the output of the data FIFO. In STIM-1/1a, all the positive pulse information on the data line to the STIM probe was determined by the data in the FIFO. This was possible because the FIFO contained 16 bit words, and there were 16 blocks of time whose state had to be determined on the data line. A couple of these states were always the same on every word cycle, such as requiring no positive pulse when the negative strobe on that line occurred. For STIM-2, however, there are more than 16 blocks of time per word of positive data line data whose state must be determined, although only 16 that vary from word to word. The wiring enhancements allow the timing PAL to override the state of the data line during the times that are the same for every word.

The last major wiring changes involved the state counter chip. The timing PAL works with a state counter chip because the 10 flip-flops in the PAL are not enough to handle the required timing variations. For STIM-1/1a, the state counter simply cycles through 16 states, the only exception being an external reset. For STIM-2, however, it is necessary to cycle through more than 16 states. The basic maximum cycle was expanded to 32 through the addition of an additional counter bit which resides in the timing PAL and is synchronized with the external counter chip. In order to terminate the cycle at numbers larger than 16 but smaller than 32, as is required by STIM-2, the timing PAL must be able to reload the external counter with zeroes at any time. This wiring enhancement was also completed.

All of the daughter board wiring enhancements just described have been designed, implemented, and tested; and all are working properly. The second major set of changes required involve the timing PAL. This had to implement basic structural changes such as resetting the external counter and the override control of the positive data for the data line and be able to execute the existing STIM-1/1a sequences in this new hardware context where additional control is required. The PAL design also had to be able to respond to the STIM-2 bit from the control register and generate the STIM-2 timing protocol in this case.

The required changes just described ran into some unanticipated problems. The major one was that it turned out that one more PAL flip-flop was required than was available to implement the changes. Above and beyond what was used previously for STIM-1/1a, the new external counter reset output required a flip-flop, the new positive data line override signal required an output, and the 5th bit to implement the new 32 bit maximum control cycle required a flip-flop. However, only two additional flip-flops were available in the 22V10 PAL being used where three were needed. The problem of finding another flip-flop without putting another chip on an already full daughter board was solved by elimination of a synchronization flip-flop for the reset input to the PAL. In order to allow this, the timing between when reset is released and the timing PAL clock starts has to be guaranteed externally now. It is physically possible to do both of these things simultaneously in a single control register write. Therefore, the C program on the PC that

drives the control register was modified so that the user could not do this in a single stroke. The time that it takes the user to issue separate commands to release the reset and initiate a single step, word step, or run command that would run the PAL clock, easily satisfies the reset time requirements before starting the PAL clock. This frees up the additional flip-flop needed. The PAL has now been re-designed and appears to be generating the STIM-1, -1a, and -2 sequence properly. However, it has yet to be tested against an actual STIM-2 circuit implementation to ensure that the interface and STIM-2 work together properly in practice.

Several things need to be done to complete the STIM-2 interface. The C control program needs to be updated to support the full set of changes in the hardware. The program on the DSP board also needs to be updated the reflect both changes and additional capabilities that are required. The PAL changes need to be fully simulated to test for pathological states that might be entered by unusual sequences of control actions. These changes need to be thoroughly documented in the circuit diagrams, PAL design files, DSP program files, and C program files. A final version of the remote converter also needs to be built. We have been operating with a breadboarded circuit which is neither convenient to move around nor robust under such circumstances. Certain aspects of the remote converter such as opto-isolation have yet to be implemented and tested. These areas will be the major targets of work in the upcoming quarters.

6. Conclusions

During the past quarter, we have begun final layout on a new set of passive recording and stimulation probes for use by external and internal personnel. These include probes for penetration studies aimed at optimizing probe tip shape to minimize penetration forces and resulting tissue damage along the electrode track. Using a combination of a deep boron diffused shank and a shallow-diffused tip, we have demonstrated the ability to form nearly ideal tips that approach the sharpness of the defining masks.

All of the problems revealed in testing the recent run of STIM-1 active probes have been corrected with simple process changes with the exception of the background currents noted on these devices. Extensive tests have been carried out to quantify and explain these currents. Both lateral and vertical parasitic bipolar transistors have been found to generate these currents in processes using moderately deep p-wells together with 10μm epitaxial thicknesses. It appears that reducing the p-well depth and increasing the epi thickness to 16μm will correct these problems and we are currently seeking to confirm this conclusion prior to another run of these probes.

The circuitry for a second-generation active probe (STIM-2) has been fabricated in a commercial foundry (MOSIS/Orbit) and has been tested. All of the circuitry is fully functional and appears to work as intended. This probe provides the ability to select eight of 64 output sites and generates drive currents for the selected sites with a range from -127μA to +127μA with a current resolution of 1μA. The circuitry operates from ±5V supplies and uses a 4MHz input clock. The external circuitry for driving these active probes has also been modified to accommodate both generations of the devices.

During the coming term, the new passive probes will be fabricated and the penetration studies will be started. In addition, additional testing will be performed on STIM-1 and layout will be completed on STIM-2 so that the fabrication of these probes can begin during the latter part of the summer.